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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/846,092	04/30/2001	Yuri V. Panchul	062097SI-1	4145

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EXAMINER	
GARBOWSKI, LEIGH M	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/846,092	PANCHUL ET AL.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,18-20,23,25-37,42-44,47 and 49-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13,18-20,25-37,42-44 and 49-55* is/are rejected.

7)☒ Claim(s) *12,23 and 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The terminal disclaimer filed on 08 October 2003 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of 6,226,776 B1 has been reviewed and is accepted. The terminal disclaimer has been recorded.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 25, 49-50 and 53-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama [U.S. Patent #5,530,843].

As per claim 1, Koyama discloses a method for converting a C-type language program to a hardware design [please review the entire document in addition to the following citations], comprising: creating an algorithmic representation in a given C-type programming language corresponding to a preliminary hardware design [column 9, lines 64-67]; and compiling the C-type programming language preliminary hardware design into a HDL synthesizable design [column 2, lines 35-38].

As per claim 25, Koyama discloses a method for converting a high-level language program to a hardware design [please review the entire document in addition to the following citations], comprising: creating an algorithmic representation in a given

high-level programming language corresponding to a preliminary hardware design [column 5, lines 15-32]; translating the high-level programming language preliminary hardware design into a C-type programming language preliminary hardware design [column 9, lines 64-67]; and compiling the C-type programming language preliminary hardware design into a HDL synthesizable design [column 2, lines 35-38].

As per claims 49-50 and 53-54, Koyama discloses a method for converting a high-level algorithmic programming language program to a hardware design description [please review the entire document in addition to the following citations], comprising: selecting a given high-level algorithmic programming language having at least one of pointers and structures, [column 9, lines 64-67]; creating an algorithmic representation in a given high-level programming language corresponding to a preliminary hardware design; [column 5, lines 15-32]; and compiling the high-level programming language preliminary hardware design into hardware-specific descriptions for a hardware implementation [column 2, lines 35-38].

Claims 1-11, 13, 18-20, 25-37, 42-44 and 49-55 are rejected under 35 U.S.C. 102(e) as being anticipated by Taylor et al. [U.S. Patent #5,603,043].

As per claim 1, Taylor et al. disclose a method for converting a C-type language program to a hardware design [please review the entire document in addition to the following citations], comprising: creating an algorithmic representation in a given C-type programming language corresponding to a preliminary hardware design [column 4, lines 35-38]; and compiling the C-type programming language preliminary hardware design into a HDL synthesizable design [column 1, lines 18-21]. As per claims 2-3, Taylor et al.

further disclose synthesizing the HDL design into a gate-level hardware representation using a synthesis program and using physical design tools to implement the gate-level representation as an actual hardware implementation [column 4, lines 43-63]. As per claim 4, Taylor et al. further disclose wherein the C-type programming language is selected from among a group of C-type programming languages [column 21, lines 19-33]. As per claim 5, Taylor et al. further disclose wherein the HDL is selected from among a group of HDLs [column 2, line 66-column 3, line 3]. As per claim 6, Taylor et al. further disclose simulating the HDL synthesizable design [column 1, lines 54-56]. As per claim 7, Taylor et al. further disclose wherein the step of compiling comprises: mapping predetermined C-type programming language expressions to functionally equivalent HDL program language expressions [column 5, lines 33-35]; assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design [column 5, lines 35-48]; and configuring in the HDL synthesizable design an interface [column 4, lines 43-63]. As per claims 8-10 and 18-20, Taylor et al. further disclose wherein a plurality of C-type functions are compiled into a plurality of executable HDL program language expressions that operate in parallel, simultaneously, sequentially in a data processing pipeline, synchronously and asynchronously [column 21, lines 3-18, 34-51; column 24, lines 1-2; column 25, line 5-column 26, line 11]. As per claim 11, Taylor et al. further disclose wherein at least one of struct [figure 24B]. As per claim 13, Taylor et al. further disclose wherein the step of compiling comprises: compiling a C-type program control flow into a HDL state machine [column 5, lines 33-35; column 24, line 55-column 25, line 2]; and assigning input/output as defined in the

C-type program to specific wires in the HDL synthesizable design [column 5, lines 35-48]; and further comprising: configuring in the HDL synthesizable design an interface [column 4, lines 43-63].

As per claim 25, Taylor et al. disclose a method for converting a high-level language program to a hardware design [please review the entire document in addition to the following citations], comprising: creating an algorithmic representation in a given high-level programming language corresponding to a preliminary hardware design [column 3, lines 5-14]; translating the high-level programming language preliminary hardware design into a C-type programming language preliminary hardware design [column 4, lines 35-38; column 5, lines 22-31]; and compiling the C-type programming language preliminary hardware design into a HDL synthesizable design [column 1, lines 18-21]. As per claims 26-27, Taylor et al. further disclose synthesizing the HDL design into a gate-level hardware representation using a synthesis program and using physical design tools to implement the gate-level representation as an actual hardware implementation [column 4, lines 43-63]. As per claim 28, Taylor et al. further disclose wherein the C-type programming language is selected from among a group of C-type programming languages [column 21, lines 19-33]. As per claim 29, Taylor et al. further disclose wherein the HDL is selected from among a group of HDLs [column 2, line 66-column 3, line 3]. As per claim 30, Taylor et al. further disclose simulating the HDL synthesizable design [column 1, lines 54-56]. As per claims 31, 36, Taylor et al. further disclose wherein the step of compiling comprises: mapping predetermined C-type programming language expressions to functionally equivalent HDL program language

expressions [column 5, lines 33-35]; and assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design [column 5, lines 35-48]; and further comprising: configuring in the HDL synthesizable design an interface [column 4, lines 43-63]. As per claims 32-34 and 42-44, Taylor et al. further disclose wherein a plurality of C-type functions are compiled into a plurality of executable HDL program language expressions that operate in parallel, simultaneously, sequentially in a data processing pipeline, synchronously and asynchronously [column 21, lines 3-18, 34-51; column 24, lines 1-2; column 25, line 5-column 26, line 11]. As per claim 35, Taylor et al. further disclose wherein at least one of struct [figure 24B]. As per claim 37, Taylor et al. further disclose wherein the step of compiling comprises: compiling a C-type program control flow into a HDL state machine [column 5, lines 33-35; column 24, line 55-column 25, line 2]; and assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design [column 5, lines 35-48]; and further comprising: configuring in the HDL synthesizable design an interface [column 4, lines 43-63]. As per claim 47,

As per claim 49, Taylor et al. disclose a method for converting a high-level algorithmic programming language program to a hardware design description [please review the entire document in addition to the following citations], comprising: selecting a given high-level algorithmic programming language having at least one of pointers and structures, [column 3, lines 5-14]; creating an algorithmic representation in a given high-level programming language corresponding to a preliminary hardware design; [column 4, lines 35-38; column 5, lines 22-31]; and compiling the high-level programming

language preliminary hardware design into hardware-specific descriptions for a hardware implementation [column 1, lines 18-21]. As per claims 50 and 54, Taylor et al. further disclose wherein the step of compiling comprises compiling the high-level algorithmic programming language preliminary hardware design into a HDL synthesizable design, the HDL is selected from among a group of HDLs [column 2, line 66-column 3, line 3]. As per claims 51-52, Taylor et al. further disclose synthesizing the HDL design into a gate-level hardware representation using a synthesis program and using physical design tools to implement the gate-level representation as an actual hardware implementation [column 4, lines 43-63]. As per claim 53, Taylor et al. further disclose wherein the high-level algorithmic programming language is selected from among the group of C-type programming languages [column 21, lines 19-33]. As per claim 54, Taylor et al. further disclose simulating the HDL synthesizable design [column 1, lines 54-56].

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sugimoto et al. [U.S. Patent #5,197,016] disclose a compiler using C. Shinde et al. [U.S. Patent #5,493,507] disclose synthesis using code generation and VHDL. Gregory et al. [U.S. Patent #5,748,488] disclose converting a hardware independent description into a logic network utilizing C. Furuichi [U.S. Patent #5,437,037] discloses simulation using compiled function description language. Fura [U.S. Patent #5,953,519] discloses generating hardware simulation models using C and HDL.

Claims 12, 23 and 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not disclose or teach a step of compiling C-type programming language structure assignment, structure function parameters, and structure function return values into HDL synthesizable expressions, in particular combination with the steps of the method from which the claims depend.

This is a continuation of applicant's earlier Application No. 08/931,148. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 703-305-9753. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

LEIGH M. GARBOWSKI
PRIMARY EXAMINER